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(52) UK CL (Edition O)
G5C CA310 CA342 CHB

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EP 0586155 A

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UK CL (Edition O) G5C CHB
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ONLINE: EDOC WPI JAPIO

(54) Active matrix display

(57) An active matrix liquid crystal display comprises a rectangular array of picture elements (1) driven by data and scan drivers (2, 3). Each picture element (4) comprises a liquid crystal display element (9) connected to the output of a unity gain buffer amplifier (11). The input of the amplifier is connected to a hold capacitor (5) and to series connected gate transistors (6a, 6b). The gates of the transistors (6a and 6b) are connected to a scan electrode (8) and the transistors are connected in series between a data electrode (7) and the input of the amplifier (11). The output of the amplifier (11) is connected to the connection between the transistors (6a, 6b).

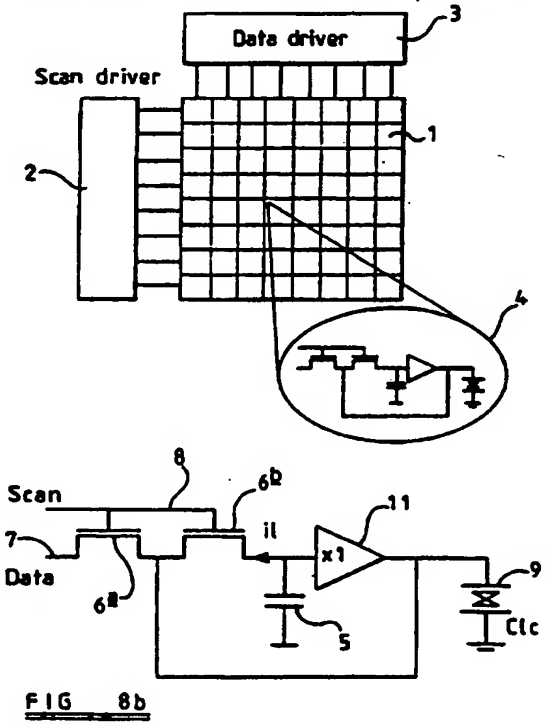


FIG 8b

GB 2 312 773 A

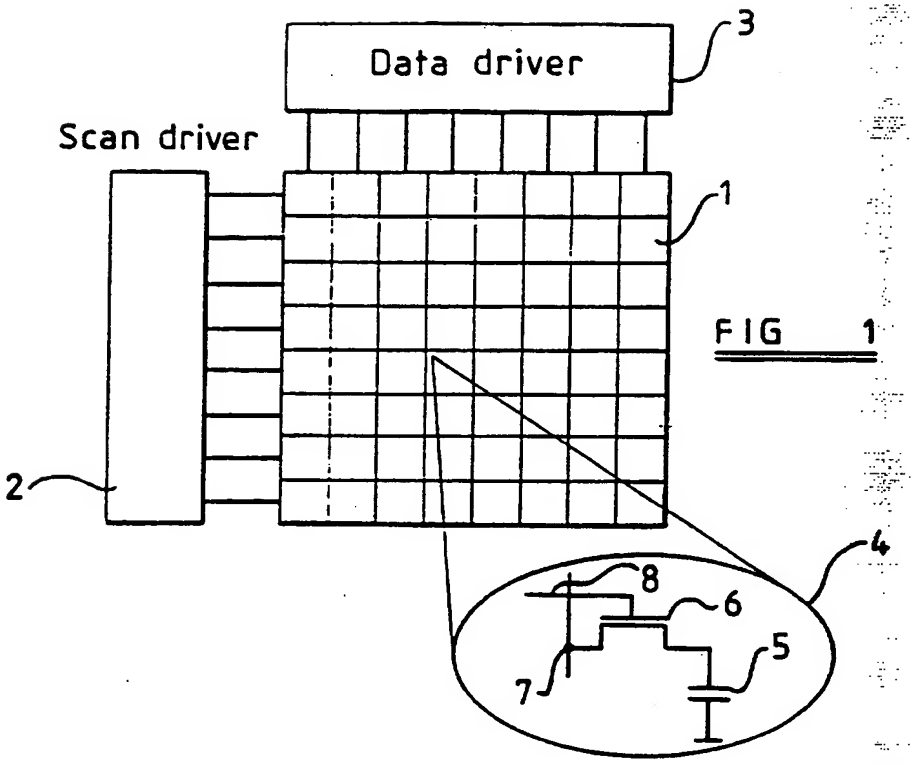


FIG 1

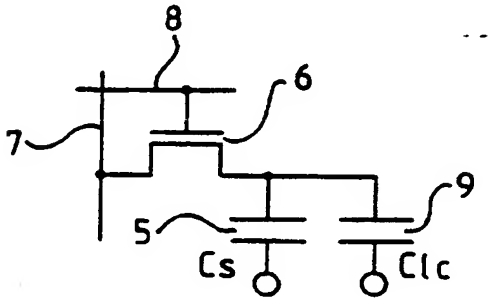


FIG 2

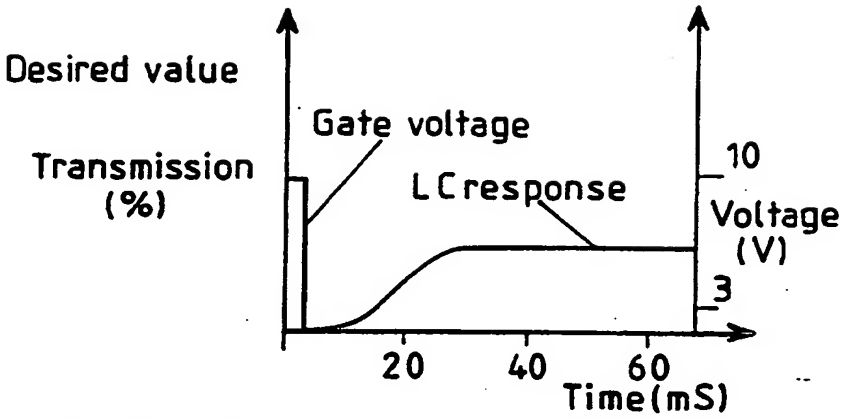


FIG 3a:LC transmission response- single impulse charging

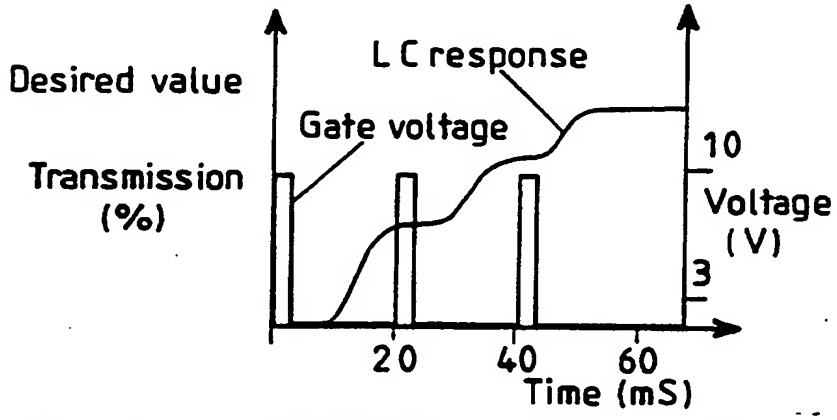


FIG 3b:LC transmission response-multiple impulse charging

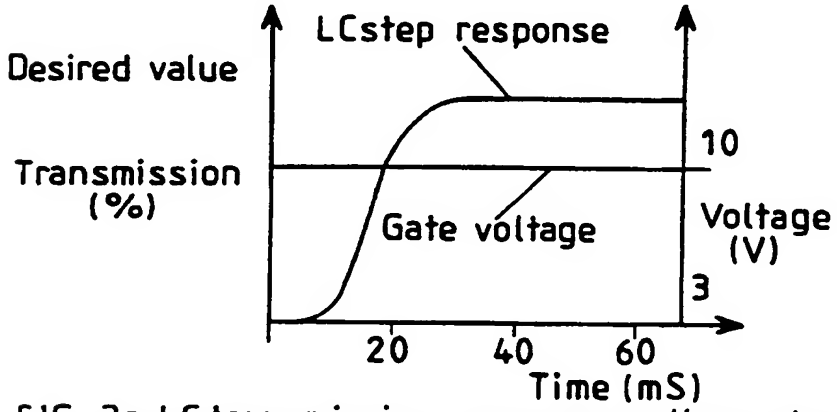


FIG 3c:LC transmission response-voltage step response

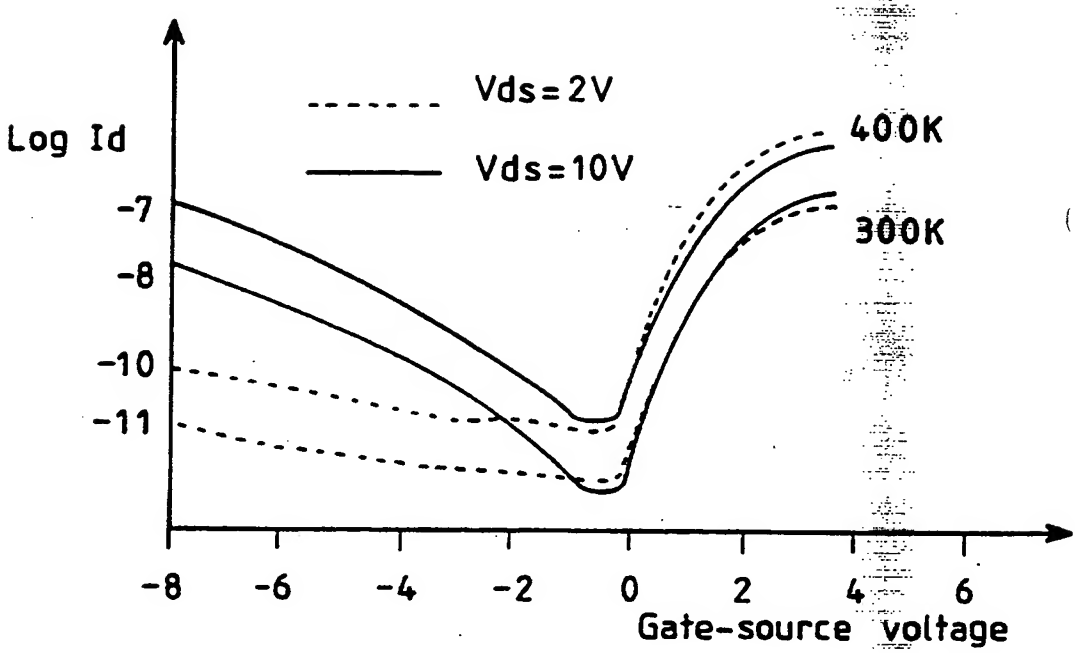


FIG 4: The leakage currents of typical polysilicon TFTs as a function of bias and temperature

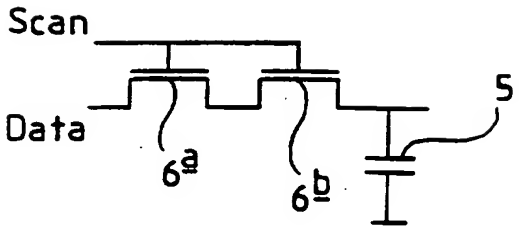


FIG 5

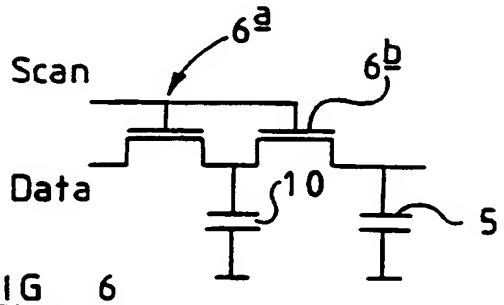


FIG 6

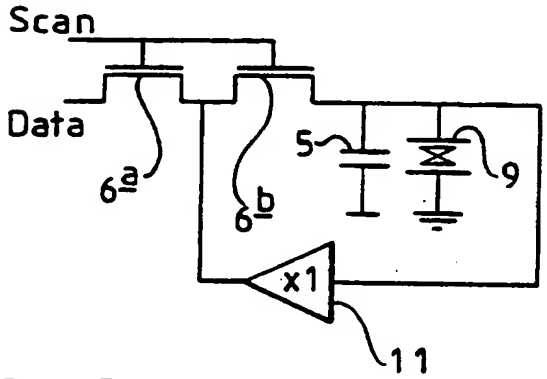


FIG 7

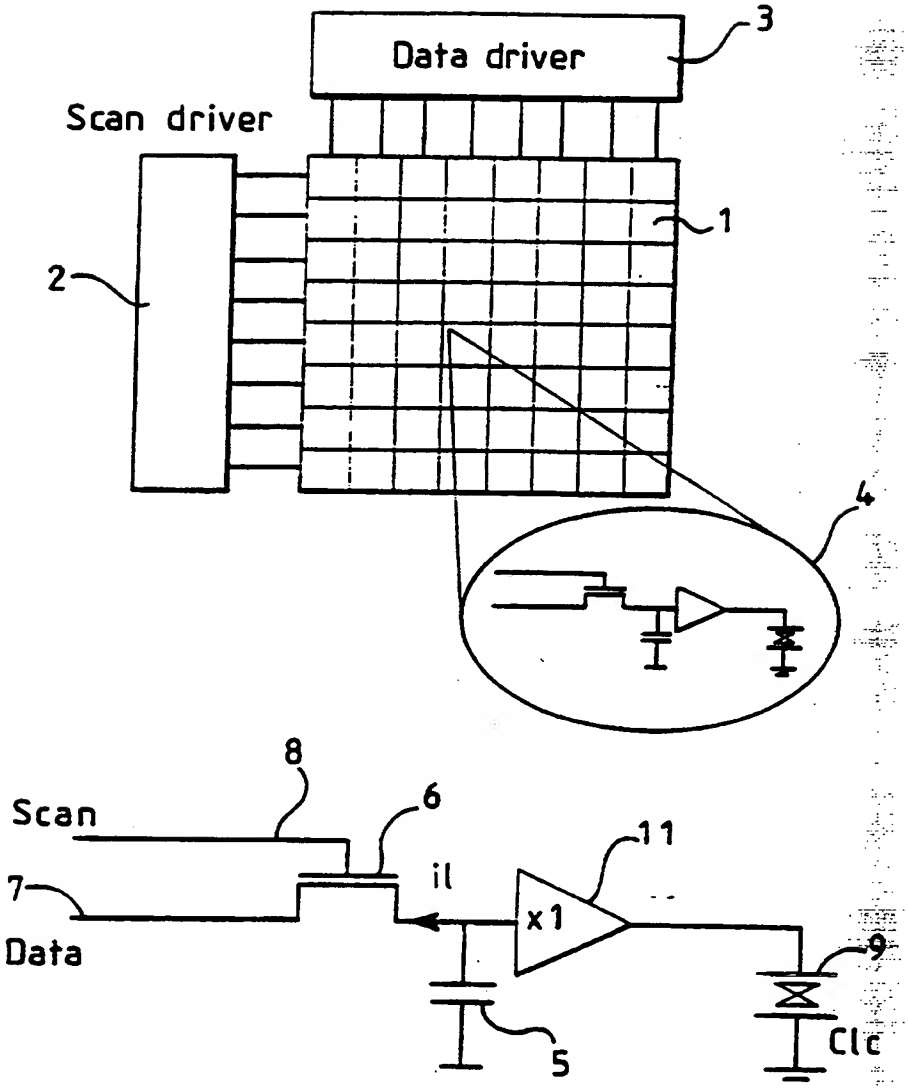
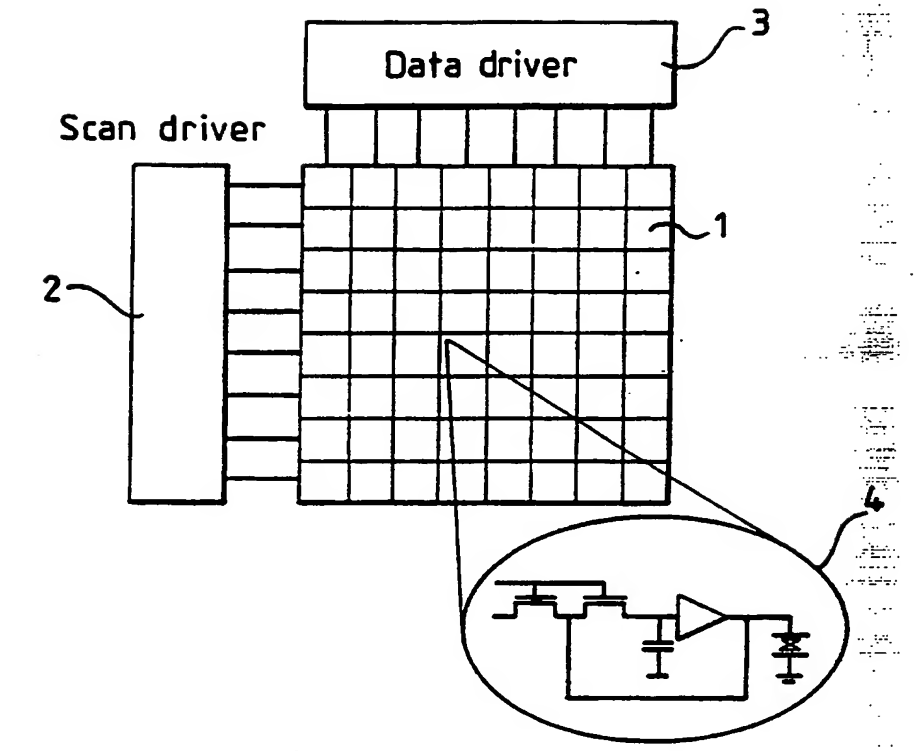


FIG 8a



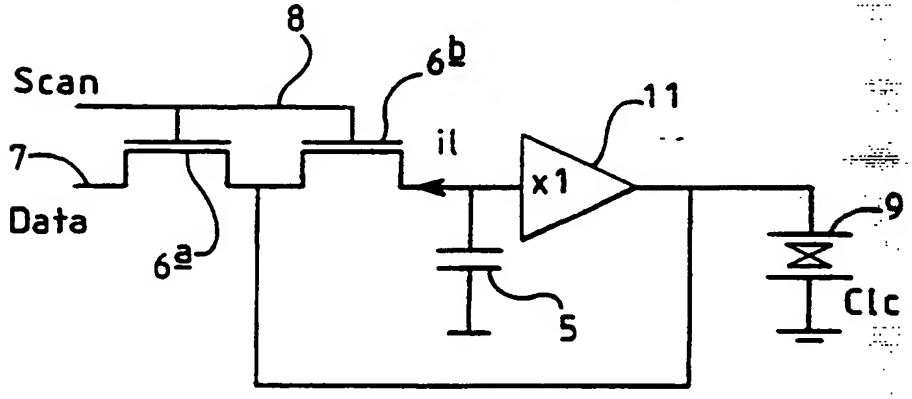


FIG 8b

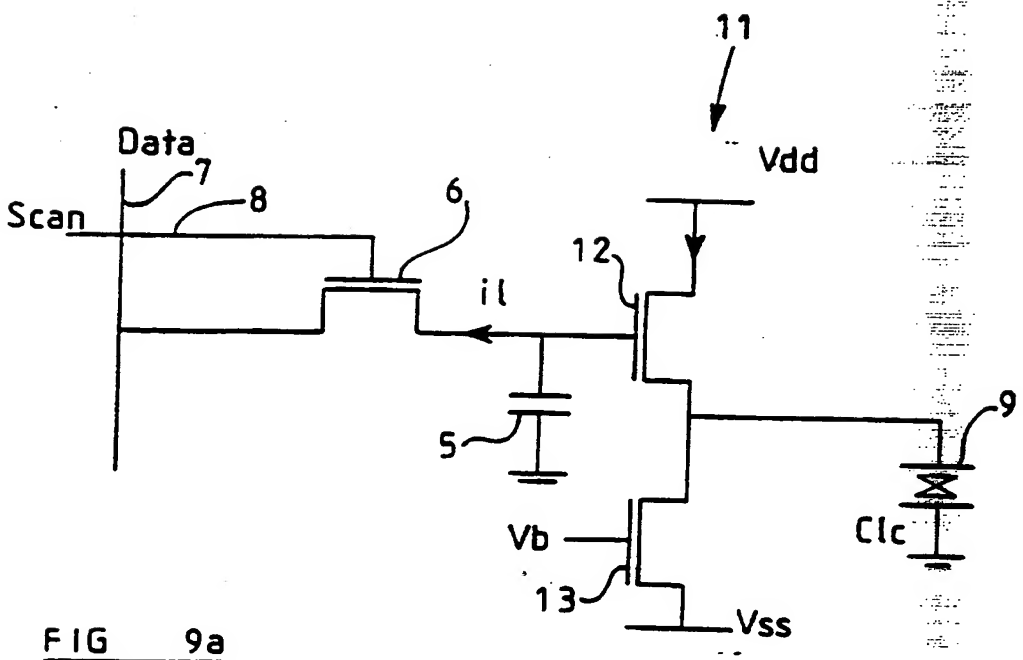


FIG 9a

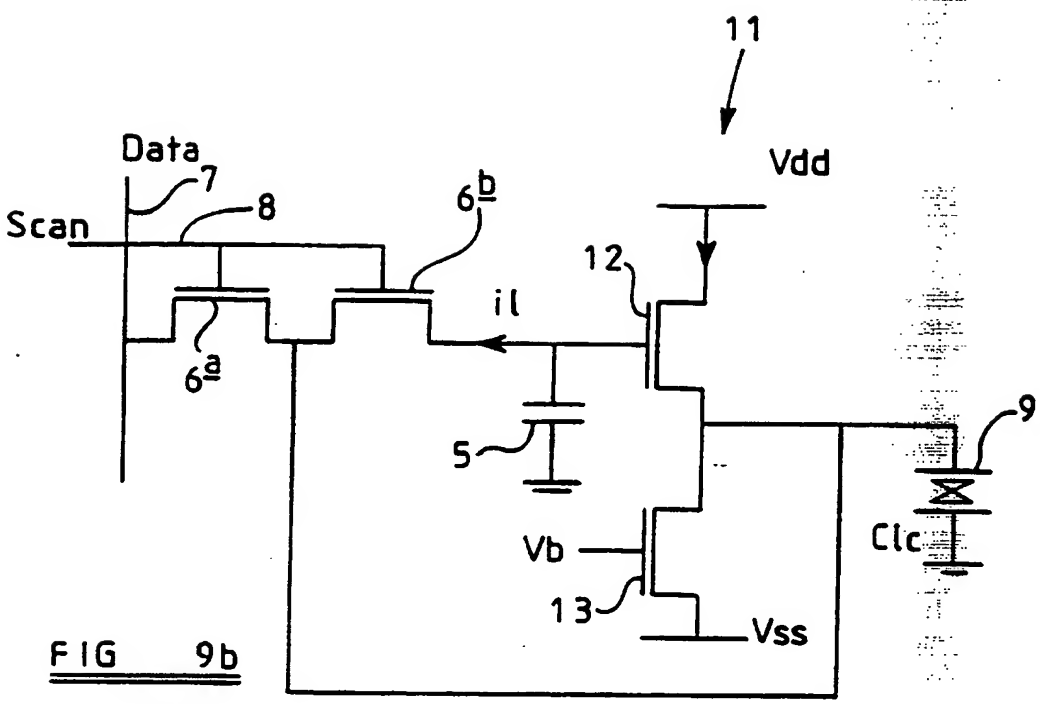


FIG 9b

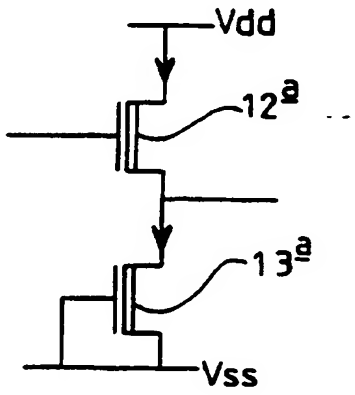


FIG 10

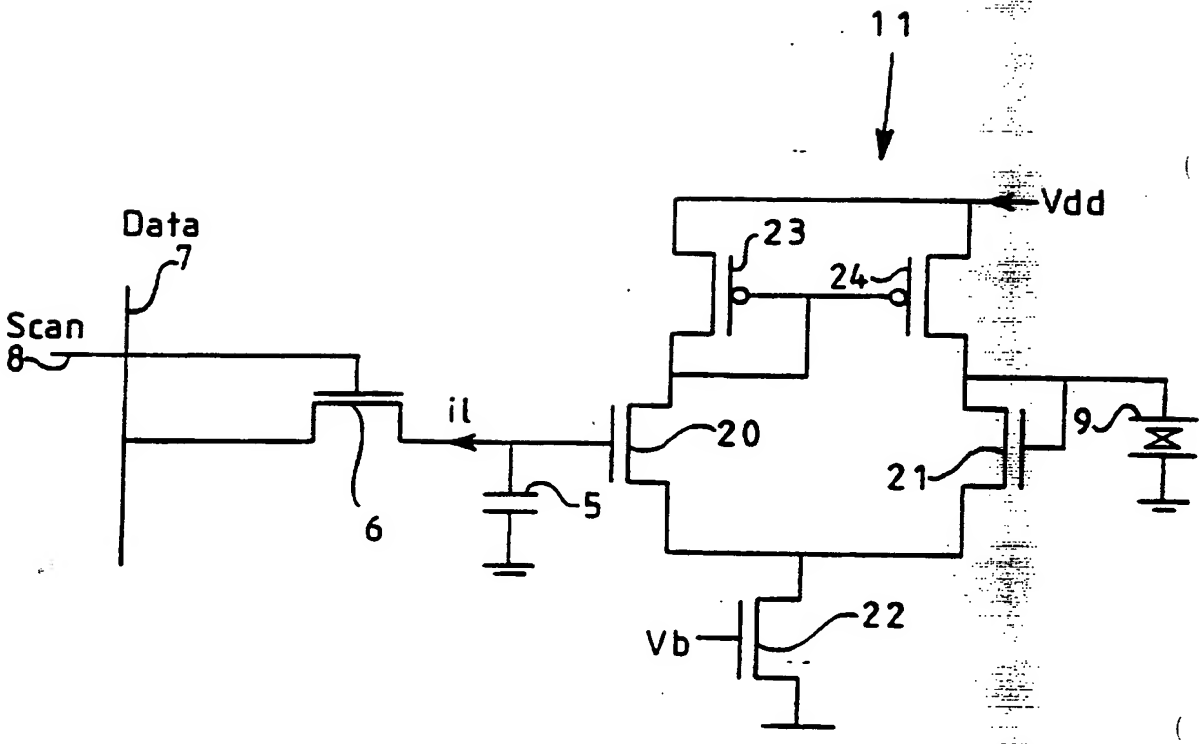


FIG 11a

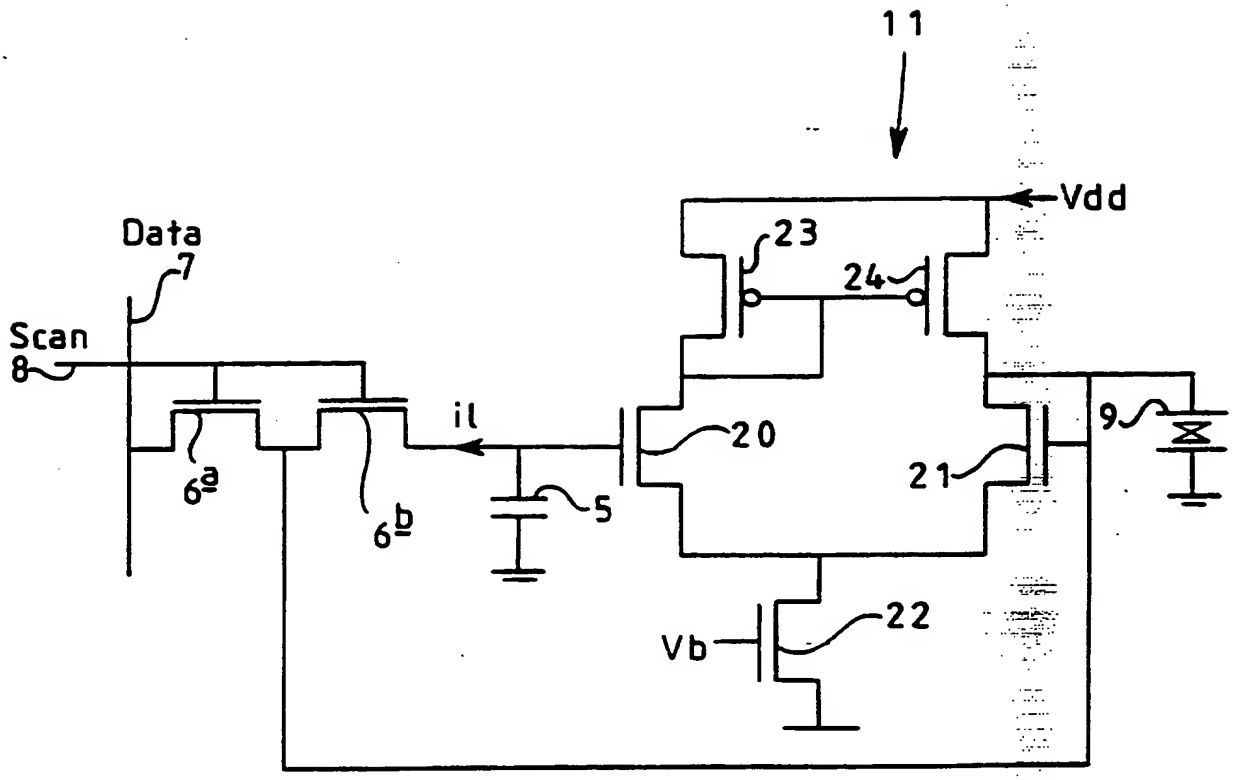


FIG 11b

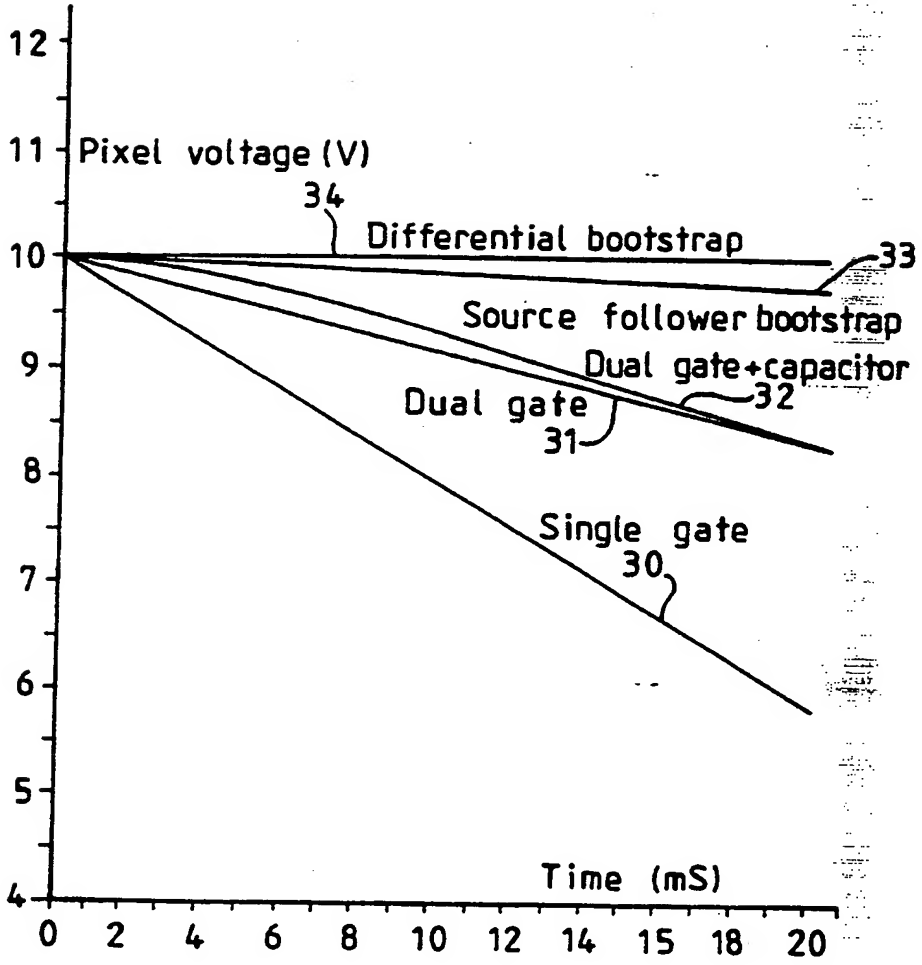

12
11
10
9
8
7
6
5
4
Pixel voltage (V)
34
Differential bootstrap
33
Source follower bootstrap
Dual gate+capacitor
32
Dual gate
31
Single gate
30
Time (mS)
0
2
4
6
8
10
12
14
15
18
20

FIG 12

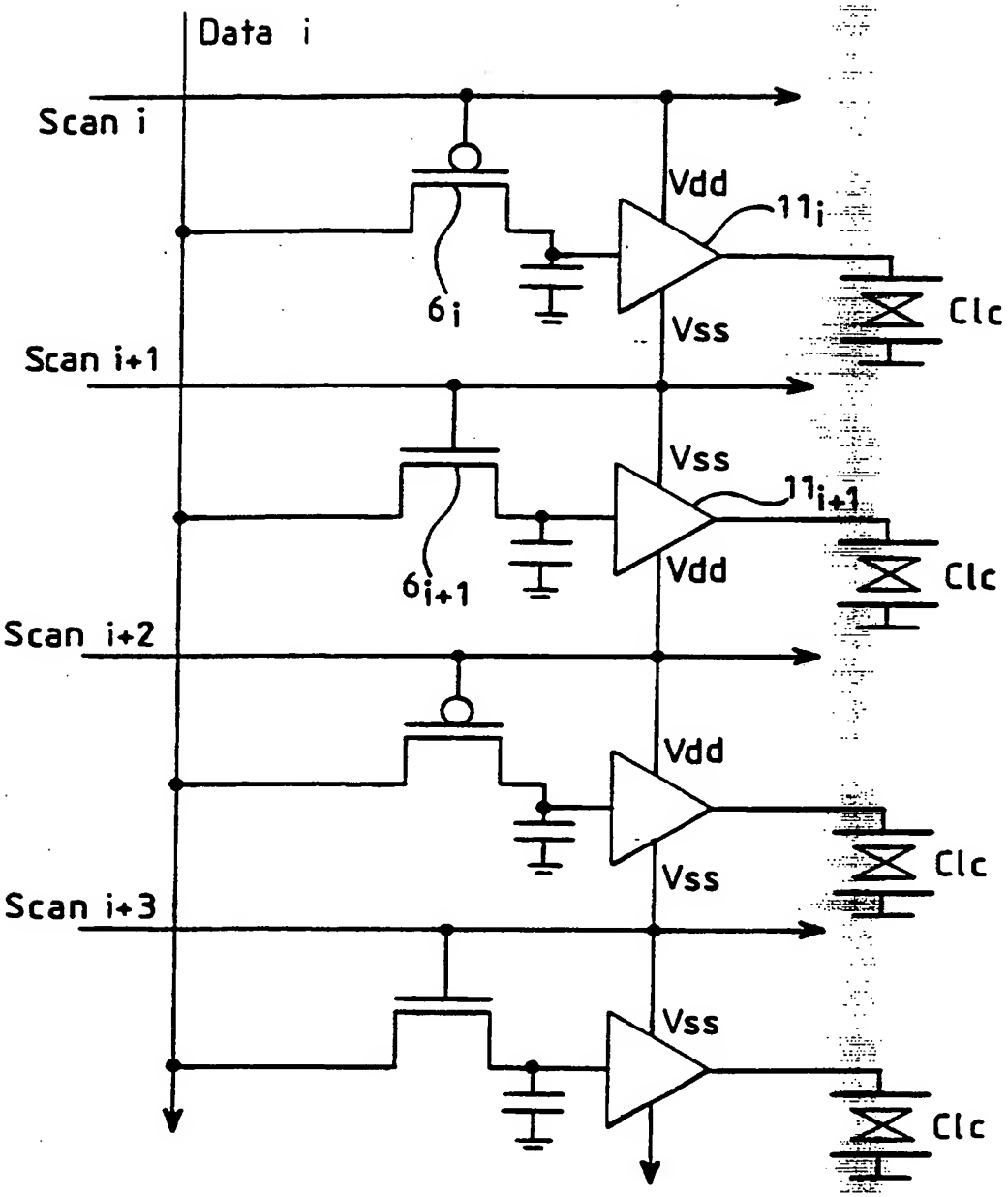

Data i
Scan i
Scan i+1
Scan i+2
Scan i+3
Vdd
Vss
11i
6i
11i+1
6i+1
Clc
Clc
Clc
Clc

FIG 13a

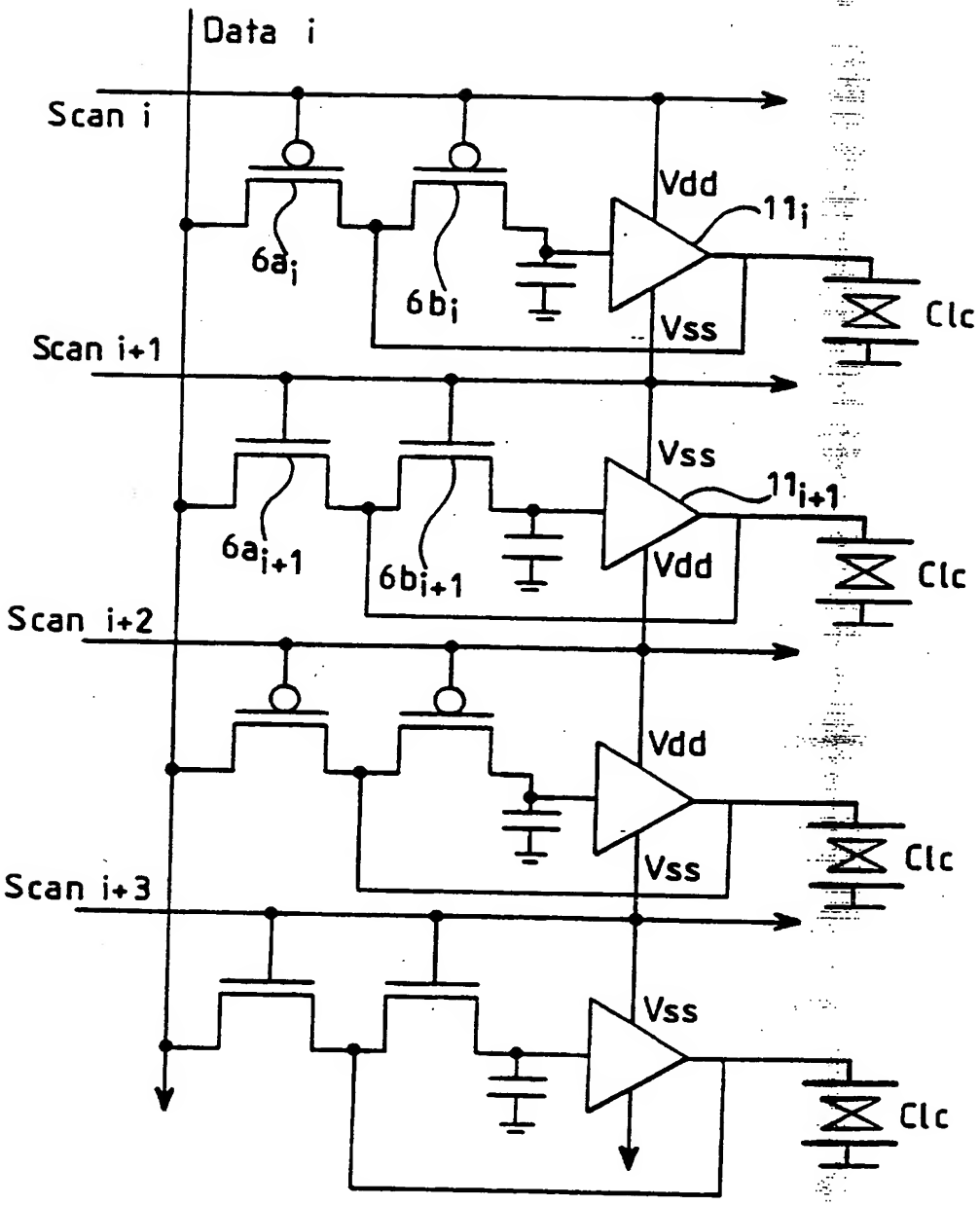

Data i
Scan i
Scan i+1
Scan i+2
Scan i+3
Vdd
Vss
11i
11i+1
6ai
6bi
6ai+1
6bi+1
Clc

FIG 13b

ACTIVE MATRIX DISPLAY.

The invention relates to active matrix displays, for instance of the liquid crystal type using low temperature polycrystalline silicon thin film transistors as active elements within the matrix.

A known type of active matrix display has active circuitry within a matrix of addressing lines in order to control the optical properties of a display material, such as liquid crystal. Figure 1 of the accompanying drawings illustrates the structure of a typical active matrix display. A regular rectangular array of active matrix elements, such as 1, is arranged as rows addressed by a scan driver 2 and columns addressed by a data driver 3. The circuit of a typical picture element or pixel is illustrated at 4.

Each pixel comprises a display element (not shown) which is effectively in parallel with a hold capacitor 5. The hold capacitor 5 is connected between the source of a thin film field effect transistor 6 and a common supply line or to the previous gate line. The gate of the transistor 6 is connected to a scan electrode 8 which is common to all of the pixels of the row and which is connected to a respective output of the scan driver 2. The drain of the transistor 6 is connected to a data electrode 7 which is common to all of the pixels of the column and which is connected to a respective output of the data driver 3.

In use, rows of pixel display data are supplied by the data driver 3 to the data electrodes 7 in synchronism with scan pulses which are supplied by

the scan driver 2 to the scan electrodes 8 in a cyclically repeating sequence. Thus, the rows of pixels are refreshed one at a time until all of the rows have been refreshed so as to complete refreshing of a frame of display data. The process is then repeated for the next frame of data.

When the scan electrode 8 of each pixel receives a scan pulse from the scan driver 2, the voltage on the data electrode 7 causes the hold capacitor 5 to be charged. When the scan pulse is removed, the transistor 6 isolates the hold capacitor 5 from the data electrode 7 so that the optical property of the associated display element corresponds to the voltage across the hold capacitor 5 until it is refreshed during the next frame.

In active matrix liquid crystal displays, the voltage stored on the hold capacitor 5 is used to modulate the optical properties of a thin layer of liquid crystal. In a known type of display, the transistors 6 forming switching elements are embodied as amorphous silicon thin film transistors. Between refresh cycles of each pixel, the dynamic behaviour of the voltage stored in the capacitor 5 is of considerable importance in determining the picture quality.

Most liquid crystal devices have a non-linear and time dependent relationship between the applied voltage and the surface charge present on the liquid crystal. This effect, known as dielectric anisotropy, implies that the effective capacitance of the liquid crystal device is a function of the applied voltage and the response time of the liquid crystal. In a conventional active matrix liquid crystal device pixel, the non-ideal liquid crystal capacitance Clc, shown at 9 in Figure 2, is in parallel with a fixed storage capacitor Cs. When the pixel is addressed by supplying a

scan pulse to the scan electrode 8, the gate voltage of the transistor 6 goes high for a relatively short time so as to allow the display to be refreshed sufficiently rapidly to avoid visible flicker. The charging time for the capacitance comprising the parallel combination of the capacitor 5 and the display element 9 is therefore sufficiently short for the voltage dependence of the liquid crystal capacitance Clc to have no substantial effect so that the capacitance Clc may be considered constant for the duration of the scan pulse. However, during the interval between scan pulses, the transistor 6 substantially isolates the capacitor 5 and the display element 9 so that the charge across the parallel combination remains substantially constant. As the liquid crystal responds to the applied voltage, the capacitance Clc changes so that final voltage across the display element is not equal to the amplitude of the charging impulse and does not therefore correspond to the data voltage which was supplied to the data electrode 7 during scanning of the pixel. In the case of a liquid crystal having positive dielectric anisotropy, the capacitance increases so that the voltage across the liquid crystal display element falls.

The effects of dielectric anisotropy are illustrated in Figures 3a to 3c of the accompanying drawings, each of which shows superimposed graphs of gate voltage and display transmission against time. Figure 3a illustrates the liquid crystal response to a single scan pulse per refresh cycle. The voltage on the data line provides the gate voltage in the form of a relatively short pulse. The desired transmission value is indicated on the left hand vertical axis but the actual transmission characteristic of the liquid crystal display element is such that a lower than expected transmission is provided. In other words, as the liquid crystal responds to the voltage, the capacitance increases and the voltage across the liquid

crystal decreases so that the transmission does not reach the desired value.

Figure 3b corresponds to Figure 3a but illustrates the effect of several refresh cycles of the pixel with the same data signal. In particular, three refresh cycles are shown. Thus, it is possible to achieve the desired transmission by applying a sequence of scan pulses to the pixel.

Figure 3c, which corresponds to Figures 3a and 3b, illustrates the effect of charging the liquid crystal capacitance from a lower impedance voltage source. This can be achieved, for example, by switching the transistor 6 on for a longer period of time so that the hold capacitor 5 and the liquid crystal capacitance Clc are charged from the respective output of the data driver 3 which has a relatively low output impedance. The liquid crystal display element therefore achieves the desired transmission value but the rate at which the display can be refreshed is greatly reduced so that undesirable visual artefacts, such as flicker, become visible.

A known technique for reducing the effects of non-ideal capacitance is to make the capacitance Cs of the hold capacitor much greater than the non-ideal liquid crystal capacitance Clc. This approach is acceptable for typical nematic materials which typically have a surface charge density of $10^{-4}C/m^2$. There are, however, liquid crystal modes which exhibit a much larger difference in surface charge density between switched states. To drive these materials using the conventional active matrix scheme would necessitate supplying this potentially large value of charge during the time that the scan line is high. Since there is not enough time for the liquid crystal material to respond during the scan time, this would

require a very large storage capacitor, a very high data voltage and a conventionally sized capacitor, or a compromise between these methods. In general, it would be impractical to consider using the conventional active matrix scheme in such circumstances because the combinations of large capacitances and/or voltages would have a disadvantageous effect on the aperture ratio and power consumption of the display. Examples of such materials include liquid crystal devices with a spontaneous polarisation, such as surface stabilised ferroelectrics, or a field-induced spontaneous polarisation, such as electroclinics, helioelectrics, deformed helix ferroelectrics, antiferroelectrics, random phases, and columnars.

In addition to the effects of dielectric anisotropy, the effect of leakage current through the thin film transistor 6 may also give rise to undesirable visual artefacts. The leakage current is that current which flows across the transistor channel when the gate voltage is below the threshold voltage. If the leakage current is too high, then the voltage across the liquid crystal element decays significantly for the frame period. As a result, the transmission characteristics of the element will change significantly between refreshes so that the display produces visible flicker.

Recent advances in thin film transistor processing technology have resulted in the development of high performance polysilicon thin film transistors. In particular, it is now possible to fabricate such transistors at temperatures which are low enough to be compatible with the glass substrates used in displays. Further, such transistors can now be made with improved drive capability compared to conventional amorphous silicon thin film transistors and may therefore be used not only within each pixel of the display but also for high speed peripheral drive

circuitry, such as in the drivers 2 and 3. The manufacturing cost of integrated displays may thus be reduced.

At the pixel level, polysilicon transistors may be made smaller than amorphous silicon transistors with the advantages that the aperture ratio can be improved and scan voltage feedthrough can be reduced. However, the leakage current of a polysilicon thin film transistor is much worse than that of an amorphous silicon thin film transistor. The off-state leakage represents one of the most variable parameters over a display panel and is highly dependent on the gate-source voltage and drain-source voltage of the transistors 6. These characteristics therefore represent a major problem in adopting polysilicon thin film transistors as switching elements in active matrix liquid crystal display panels.

Figure 4 of the accompanying drawings shows graphs of drain current on a logarithmic scale against gate-source voltage for two different device temperatures and two different drain-source voltages. Decreasing the drain-source voltage provides an exponential reduction in the leakage current at all temperatures. Thus, as is known, it is possible to reduce leakage current by field reduction at the drain of the transistor. F. Okumura and K. Sera, A.M.L.C.D., p24-27 (1994) discloses several techniques for achieving this, such as Lightly Doped Drain (LDD) Structures, Offset Gate (OG) Structures, Active Gates (AG) and Multiple Gates.

LDD and OG structures reduce the field at the drain but also have a deleterious effect on the on-state current and hence the speed of such devices. This is not ideal for integrated displays because it requires different processes to be used for the pixel transistors, where off-current

is crucial, and for the drivers, where high speeds are crucial. The use of extra processing steps is undesirable and may increase the cost of manufacture.

An alternative technique is the use of multiple gates which amounts to using two or more thin film transistors in series as illustrated in Figure 5 of the accompanying drawings. The single gate transistor 6 of the arrangement shown in Figures 1 and 2 is replaced by a multiple gate transistor equivalent to the transistors 6a and 6b of Figure 5. However, there may not be sufficient field reduction across the devices to prevent excess leakage current so that this technique has often been applied together with the LDD technique.

Another known technique shown in Figure 6 of the accompanying drawings is to use an additional hold capacitor 10 at the junction of the multiple gate structure, which is effectively between the transistors 6a and 6b. However, it is doubtful whether such an arrangement will provide sufficient hold times to allow the use of polysilicon thin film transistors in displays without undesirable visual artefacts.

Figure 7 of the accompanying drawings illustrates another technique for extending the hold time over several frames as disclosed in Japanese laid-open Patent Application No. 5-142573. This technique involves "boot-strapping" by connecting a unity voltage gain amplifier 11 with its input to the capacitor 5 and the display element 9 and its output to the junction between the transistors 6a and 6b. Thus, the voltage across the capacitor 5 and the display element 9 appears at the junction of the series-connected thin film transistors 6a and 6b. If the buffer amplifier 11 were ideal and drew no charge from the capacitor 5 and the

capacitance of the display element 9, leakage from the liquid crystal would be eliminated.

Although the techniques described with reference to Figures 5 to 7 attempt to deal with the problem of leakage current, none of them deals with the problem of dielectric anisotropy in the liquid crystal of the display element 9.

According to the invention, there is provided an active matrix display as defined in the appended Claim 1.

Preferred embodiments of the invention are defined in the other appended claims.

It is thus possible to provide a display in which the undesirable effects of liquid crystal dielectric anisotropy are substantially reduced or eliminated. The refresh speed of the display may be increased and visual artefacts such as flicker can be reduced. For display elements using other technologies, the hold capacitor is substantially isolated from any undesirable effects which might otherwise be caused by the display element. It is also possible to reduce or eliminate the effects of leakage currents of semiconductor devices in the pixels. Such devices may be made using the same processing steps at the pixels and at drivers integrated with the display so that manufacturing costs are not substantially increased.

In a preferred embodiment of the invention, an active buffer is provided at each pixel in an active matrix display. The active buffer is disposed between a hold capacitor at the input and a liquid crystal cell at the

output. Further, a feedback loop may be connected from the output of the buffer to a junction of two series-connected polysilicon thin film transistors which act as pass gates from a data line to the hold capacitor. The hold capacitor, which can be of relatively small value, is charged during each row scan period and provides a voltage reference to the input of the buffer. The buffer then drives the liquid crystal cell for the remainder of the frame period with a constant voltage. Using this arrangement, it is possible to drive materials with very high surface charge density values since the charge is supplied from the buffer over a very much longer time period. The need to use high voltages and/or large hold capacitors is therefore eliminated with consequent benefits in terms of power consumption and/or aperture ratio.

If two series-connected thin film transistors are used as the data switches, then it is possible to connect the output of the buffer to the midpoint of these transistors in order to boot strap the inner thin film transistor. The active buffer tracks the voltage on the hold capacitor and simultaneously drives the liquid crystal capacitance and the junction between the past transistors. Under this condition, with an ideal buffer, the drain-source voltage of the inner transistor is substantially zero and hence the leakage current is substantially eliminated.

The invention will be further described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a schematic diagram of a known active matrix display;

Figure 2 is a diagram of an active matrix element of the display of Figure 1;

Figures 3a to 3c illustrate the effects of liquid crystal dielectric anisotropy for different gating waveforms;

Figure 4 illustrates leakage current against bias voltage for a typical polysilicon thin film transistor;

Figure 5 is a diagram illustrating a first known modification of an active matrix display for reducing leakage current;

Figure 6 is a diagram illustrating a second known technique for reducing leakage current;

Figure 7 is a diagram illustrating a third known technique for reducing leakage current;

Figures 8a and 8b are schematic diagrams of active matrix liquid crystal displays constituting embodiments of the present invention;

Figures 9a, 9b, 10, 11a and 11b are circuit diagrams showing different types of amplifiers for use in the displays of Figures 8a and 8b;

Figure 12 is a graph of pixel voltage against time in milliseconds illustrating the effects of leakage current for different active matrix pixel circuits; and

Figures 13a and 13b are diagrams illustrating the use of scan lines to power active circuitry at the pixels.

Like reference numerals refer to like parts throughout the drawings.

The active matrix liquid crystal display shown in Figure 8a is of the same general type as that shown in Figure 1. However, the active circuitry for each pixel differs in that there is provided a buffer amplifier 11 having unity voltage gain. The input of the amplifier 11 is connected to the source of the transistor 6 and to the hold capacitor 5 whereas the output of the amplifier 11 is connected to the liquid crystal display element 9. The amplifier 11 has a very high input impedance and a relatively low output impedance. The active circuitry at each pixel and the scan and data drivers 2 and 3 may comprise polysilicon thin film transistors so that all of the circuitry is made using the same manufacturing process steps.

When the pixel is addressed by applying a scan pulse to the scan electrode 8, the transistor 6 is switched on so that the hold capacitor 5 charges to the voltage which is present on the data electrode 7. Between scan pulses on the electrode 8, the transistor 6 is switched off. The output of the amplifier 11 follows the voltage across the capacitor 5 and supplies this voltage to the display element 9. The current supplied to the input of the amplifier 11 is negligible so that discharge of the capacitor 5 and hence decay of the voltage across the capacitor 5 is much slower than with the known arrangements described hereinbefore.

The output impedance of the amplifier 11 is relatively low so that the display element 9 is effectively voltage driven. Accordingly, the voltage across the display element 9 remains substantially constant despite the variable liquid crystal capacitance Clc. The liquid crystal is therefore subjected to a voltage step which is applied for the entire frame refresh time. It may therefore be possible to increase the frame refresh rate of the display. Further, because of the reduced charge drain on the

capacitor 5, the capacitance of the capacitor 5 may be reduced so as to reduce the area required for this component.

The effect of liquid crystal dielectric anisotropy is substantially reduced or eliminated. The display element can achieve the desired transmission value without the need for multiple or extended addressing. Visual artefacts such as flicker can be made substantially imperceptible. The refresh rate may be increased. Alternatively, for applications requiring a lower refresh rate, the desired value of transmission of the pixels can be retained for longer periods between refreshes.

The active matrix liquid crystal display shown in Figure 8b differs from that shown in Figure 8a in that the transistor 6 is replaced by series-connected transistors 6a and 6b, for instance of the multiple gate type shown in Figure 5. The output of the amplifier 11 is connected to the connection between the source of the transistor 6a and the drain of the transistor 6b.

The connection between the source of the transistor 6a and the display amplifier 11 provides a path for initial charging from the dataline. After scanning of the line containing the pixel, the output of the amplifier 11, and hence the drain of the transistor 6b, are at the same voltage as the capacitor 5. The source-drain voltage across the transistor 6b is substantially equal to zero so that the leakage current il is substantially equal to zero.

There are a number of possible implementations of the unity gain buffer amplifier 11 and the choice will be dependent on a number of considerations including area, efficiency and fault tolerance.

Figures 9a and 9b illustrate one type of buffer amplifier 11 in the form of a source-follower. The source follower comprises enhancement transistors 12 and 13 connected in series between supply lines Vdd and Vss. The gate of the transistor 12 forms the input of the amplifier connected to the capacitor 5 whereas the source of the transistor 12 forms the output of the amplifier. The gate of the transistor 13 is connected to a bias voltage Vb and forms a constant current source load for the transistor 12.

The current requirements of the source follower shown in Figures 9a and 9b are extremely small since it is only required to supply the current required to track changes in the capacitance Clc of the liquid crystal display element 9 and, in the embodiment shown in Figure 9b, the current necessary to compensate leakage.

As shown in Figure 10, the source-follower may be embodied by means of depletion transistors 12a and 13a. In this case, the gate of the transistor 13a is connected to the source so as to form the constant current generator. Thus, the bias voltage Vb is not required so that an extra supply wire is avoided.

Figures 11a and 11b show another type of unity gain buffer amplifier based on a differential amplifier using polysilicon enhancement thin film transistors. The amplifier comprises differential input transistors 20 and 21 in the form of a "long-tail pair" and a current source comprising a transistor 22 whose gate is connected to receive a bias voltage Vb. The drain of the transistor 20 is connected to the input of a current mirror whose output is connected to the drain of the transistor 21. The current mirror comprises transistors 23 and 24 of opposite conduction type to

the transistors 20 to 22. The non-inverting input of the differential amplifier comprises the gate of the transistor 20 which is connected to the hold capacitor 5. The gate of the transistor 21 forms an inverting input which is connected to the output of the amplifier formed by the connection between the drains of the transistors 21 and 24. The transistors are run at subthreshold currents so that the closed loop gain of the amplifier is very close to unity. During operation of the embodiment shown in Figure 11b between scan pulses, the voltage difference across the channel of the transistor 6b is equal to the input offset voltage of the amplifier 11 and this is of very small value.

Figure 12 illustrates the hold capacitor voltage decay against time for the arrangements described hereinbefore. Curve 30 illustrates the performance of the circuit shown in Figure 1 and illustrates that the pixel voltage decays relatively rapidly. For a standard video display with a frame refresh period of the order of 20 milliseconds, the pixel voltage decays from the nominal 10 volts to approximately 6 volts. Curve 31 illustrates the performance of the circuit shown in Figure 5 whereas curve 32 illustrates the performance of the circuit shown in Figure 6. In the 20 millisecond refresh period, the pixel voltage decays from 10 volts to approximately 8.5 volts. These voltage decays result in perceptible visual artefacts.

Curve 33 illustrates the performance of the circuits shown in Figures 8a, 8b, 9a, 9b and 10 and illustrates that the voltage decay during the refresh period is relatively small and less than 0.5 volts. Curve 34 illustrates the performance of the circuits shown in Figures 11a and 11b, for which the pixel voltage decays by a negligible amount during the 20 millisecond refresh period.

It is thus possible to provide an active matrix display in which the effects of liquid crystal dielectric anisotropy are substantially eliminated so that there are no perceptible visual artefacts in the display. The effects of gating transistor leakage current are greatly reduced or substantially eliminated. It is thus possible to use polysilicon thin film transistors in active matrix displays of improved performance so that no extra processing steps are necessary during manufacture.

A possible disadvantage of the presence of the buffer amplifiers 11 at the pixels is the need to provide supply voltages to the supply lines Vdd and Vss. Any extra wiring could have a significant effect on the aperture ratio of high resolution displays and would introduce a greater risk of bridging faults within the electrode matrix. However, Figures 13a and 13b illustrate arrangements which make additional wiring unnecessary.

Figures 13a and 13b show part of one column of pixels of an active matrix display. Each pixel is of the type illustrated in Figures 8a and 8b. However, the polarities of the active devices of the pixel in adjacent rows are opposite. Thus, the transistor 6_i is of p type, the transistor 6_{i+1} is of n type, and so on. For the p type gate transistors such as 6_i, the transistors are on when the scan line i is negative and are off when the scan line i is positive. For the n type transistors such as 6_{i+1}, the transistors are on when the scan line i+1 is positive and off when the scan line is negative. Thus, alternate scan lines are negative in the absence of a scan pulse whereas the remaining scan lines are positive in the absence of a scan pulse. The scan lines can thus be used to supply power to the amplifiers 11_i, 11_{i+1} with the amplifier supply lines Vdd and Vss connected as shown in Figures 13a and 13b. The active circuitry at each pixel is thus powered whenever the scan lines above

and below the cell are in their quiescent state i.e. during the whole time between refreshing of the corresponding pixel rows. It is therefore possible to power the amplifiers without the need for extra wiring.

The arrangement shown in Figure 13b differs from that shown in Figure 13a in that each of the transistors such as 6_i and 6_{i+1} is replaced by a pair of series-connected transistors $6a_i$, $6b_i$ and $6a_{i+1}$ and $6b_{i+1}$. The gates of the transistors $6a_i$ and $6b_i$ and connected to the scan line i and the source of the transistor $6a_i$ and the drain of the transistor $6b_i$ are connected together and to the output of the amplifier 11_i.

CLAIMS

1. An active matrix display comprising a plurality of picture elements, each of which comprises a gate having a data input connected to a data electrode and a scan input connected to a scan electrode, a hold capacitor connected to the output of the gate, a buffer amplifier having an input connected to the hold capacitor, and a display element connected to the output of the buffer amplifier.

2. A display as claimed in Claim 1, in which each display element comprises a liquid crystal display element.

3. A display as claimed in Claim 1 or 2, in which the gate and the amplifier comprise polysilicon active devices.

4. A display as claimed in Claim 3, in which the active devices comprise polysilicon thin film transistors.

5. A display as claimed in any one of the preceding claims, in which the amplifier has unity voltage gain.

6. A display as claimed in any one of the preceding claims, in which the gate comprises first and second semiconductor switches connected in series and in which the output of the amplifier is connected to a circuit node between the first and second switches.

7. A display as claimed in Claim 6, in which each of the first and second switches comprises a transistor.

8. A display as claimed in any one of the preceding claims, in which the amplifier comprises a source follower.

9. A display as claimed in Claim 8, in which the source follower has a constant current source load.

10. A display as claimed in any one of Claims 1 to 7, in which the amplifier comprises a differential amplifier having a non-inverting input connected to the hold capacitor and an inverting input connected to the output.

11. A display as claimed in Claim 10, in which the differential amplifier comprises first and second transistors having a common source load.

12. A display as claimed in Claim 11, in which the common source load is a constant current generator.

13. A display as claimed in Claim 11 or 12, in which the amplifier comprises a current mirror connected to the drains of the first and second transistors.

14. A display as claimed in any one of the preceding claims, in which the picture elements are arranged as a plurality of rows with the scan inputs of the picture elements of each row being connected to a respective common scan electrode, the amplifiers of the picture elements of each row having power supply terminals connected between the common scan electrodes of an adjacent pair of rows.

15. A display as claimed in Claim 14, in which the gates of the picture elements of adjacent rows comprise semiconductor devices of opposite conductivity types.

16. A display substantially as hereinbefore described with reference to and as illustrated in Figures 8a, 8b, 9a, 9b, 10, 11a, 11b, 13a and 13b of the accompanying drawings.

The Patent Office

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Application No: GB 9609064.2
Claims searched: 1 to 16

Examiner: Mr.G.M Pitchman
Date of search: 24 July 1996

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): G5C (CHB)

Int Cl (Ed.6): G02F 1/136 G09G 3/36

Other: ONLINE: EDOC WPI JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
X	EP 0586155 A2 (SHARP)-see abstract, claim 1 and figure 1	1, 2

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
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